Remarks/Arguments

The Examiner is thanked for the thorough examination and search of the subject patent application.

Claims 1, 4, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 29, 30, 91, 96-99, 101-103 and 108-139 are pending; Claims 1, 9, 15, 22, 97, 119, 126, 129 and 136 have been currently amended. Claims 4, 29, 30 and 115 have been withdrawn; Claims 2, 3, 5, 6, 8, 13, 14, 16, 20, 23, 24, 26, 28, 31-90, 92-95, 100 and 104-107 have been canceled. No new matter is believed to have been added.

Response to Claim Objections

Reconsideration of the objection to Claims 1, 7, 91, 96-97, 113-114, 117, and 123-128 is respectfully requested in view of Amended Claims 1, 9, 15, 97, 119, 126, 129, and 136 and in accordance with the following remarks.

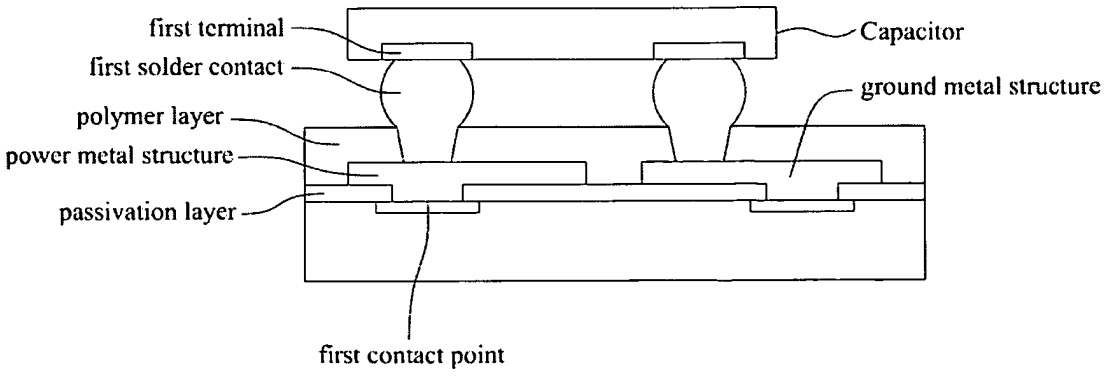
Fig. 3 shows the first terminal 34 of the capacitor 38 directly over the first contact point, labeled V_{DD}, at the bottom of the opening in the passivation layer 18. Please see the description of Fig. 3 on pages 10-11 of the Specification.

Response to Claim Rejections under 35 U.S.C. 112

Reconsiderations of Claims 1, 7, 91, 96, 97, 113, 114, 116, 117 and 123-128 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention are requested based on the following remarks.

The Examiner considers that "In base claim 1, line 25 recites "a capacitor over said passivation and directly over said first contact point" and lines 27-28 also require "a first solder contact directly over said first contact point and between said capacitor and said power metal structure". Given that the "solder contact" is "directly over said first contact point", it is not possible for the capacitor to also be "directly over said first contact point"." *~ See lines 7-12 on page 3, in the last Office Action mailed May 12, 2009 ~*

In response to the Examiner's opinion, please see the following drawing:



In the above drawing, both a first solder contact and a first terminal of a capacitor are directly over a first contact point at a bottom of an opening in a passivation layer. Therefore, given that a solder contact is directly over a first contact point, it is possible for a capacitor to also be directly over the first contact point.

For the above reasons, withdrawal of the Claim Rejection under 35 U.S.C. 112, second paragraph, to Claims 1, 7, 91, 96, 97, 113, 114, 116, 117 and 123-128 is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 1, 4, 7, 91, 96, 97, 113-117 and 123-128

==========

As currently amended, independent Claim 1 is recited below:

1. An integrated circuit chip comprising:
   a semiconductor substrate;
   a transistor in and on said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a second contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein a second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;

a power metal structure over said passivation layer and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening, wherein said power metal structure comprises a copper layer, and wherein said power metal structure has a first region used to be wirebonded thereto for connection made to a next level of packaging;

a ground metal structure over said passivation layer and on said second contact point, wherein said ground metal structure is connected to said second contact point through said second opening, wherein said ground metal structure comprises a copper layer, and wherein said ground metal structure has a second region used to be wirebonded thereto for connection made to said next level of packaging;

a capacitor over said passivation layer and directly over said first contact point;

a first solder contact directly over said first contact point and between a first terminal of said capacitor and said power metal structure, wherein said first solder contact connects said first terminal to said power metal structure; and

a second solder contact between a second terminal of said capacitor and said ground metal structure, wherein said second solder contact connects said second terminal to said ground metal structure.

==========

Reconsiderations of Claims 1, 7, 91, 96, 97, 113, 114, 116, 117 and 123-128 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 1 patentably distinguishes over the citation by Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980).

The Examiner considers that in col. 8, lines 21-24 in Lin's teaching, Lin's structure directly above 16 shown on the right side can be deemed as a power metal structure and Lin's structure directly above 16 shown on the left side can be deemed as a ground metal structure. ~ *See lines 6, 7, 11 and 12 on page 5, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion. In col. 8, lines 21-27, in U.S. Pat. No. 6,303,423, Lin discloses that "A pad can, for instance, be used as a flip chip pad. Other pads can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in FIG. 2: pad 26 can serve as a flip chip pad, pad 28 can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical signal bus."

Based on the above disclosure, one of ordinary skill in the art would consider that a pad can be used for power connection, ground connection or signal connection, but would not anticipate that a capacitor has two terminals connected to a power metal structure and a ground metal structure, respectively, as currently claimed in Claim 1 because Lin fails to teach, hint or suggest what kind of connections can be made to terminals of Lin's capacitor 54.

The Examiner considers that "It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi so that said power metal structure and said ground metal structure has a first region and a second regions, respectively, used to be wirebonded thereto for connection made to a next of packaging. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing routing for interconnects to contact pads that are closer to the periphery of the semiconductor substrate (compared to the capacitor, thus allowing flexibility of placing the capacitor in a central location on the semiconductor substrate, as shown in Figure 3b of Nakanishi), while still being able to connect to the ground or power of next level of packaging without excessive wirebond length and a high electrical conductivity metal, like copper, which improves electrical performance and which allows long interconnect length, to connect to next level of packaging." ~ *See line 12 of page 6 through line 1 of page 7, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion because there is no motivation to make Lin's capacitor 54 to be connected to a wirebond through a routing interconnect in view of Nakanishi et al.'s teaching. Nakanishi et al.'s capacitor 8 is an external capacitor having two terminals connected to an external circuitry through Nakanishi et al.'s wiring traces 5. However, Lin's capacitor 54 is an internal capacitor having two terminals both connected down to underlying devices through two openings in a passivation layer 18, but not to an external circuitry. The two terminals of Lin's capacitor 54 are suggested to be directly over contact points at bottoms of the two openings in the passivation layer 18 without any rerouting trace because this is the minimum connection

to the underlying devices. Therefore, Nakanishi et al.'s wiring traces 5 or Nakanishi et al.'s wirebonding wires 12 are not believed to be applied to Lin's device because Lin fails to teach, hint or suggest Lin's capacitor 54 is an external capacitor, like Nakanishi et al.'s capacitor 8, having at least a terminal connected to an external circuitry.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 1 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 4, 7, 91, 96, 97, 113-117 and 123-128 patentably define over the prior art as well.

Response to Claims 9-12, 98, 99 and 118-122

==========

As currently amended, independent Claim 9 is recited below:

9. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein said passivation layer comprises a nitride;

a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and over said second contact pad;

a solder contact between a terminal of said capacitor and said second contact pad, wherein said solder contact connects said terminal to said second contact pad; and

electroplated copper between said solder contact and said second contact pad.

==========

Reconsiderations of Claims 9-12, 98, 99 and 118-122 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 9 patentably distinguishes over the citation by Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980).

The Examiner considers that "As for the thickness of the gold layer is considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer ....." ~ *See lines 1-7 on page 12, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion because a gold layer having a thickness greater than 1 micrometer is not believed to involve routine optimization. If the Examiner does consider that a gold layer having a thickness greater than 1 micrometer involves routine optimization, showing a reference disclosing the routine optimization of a gold layer having a thickness greater than 1 micrometer is respectfully requested.

The Examiner considers that "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *~ See lines 14-19 on page 12, in the last Office Action mailed May 12, 2009 ~*

In response to the Examiner's opinion, the "electroplated copper" has a specific micro-structure that can be identified in a final product by the grain size using a TEM cross-section or by the composition analysis using Energy-Dispersive X-ray (EDX) spectroscopy or X-ray fluorescence.

==========

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., In re Garnero, 412 F.2d 276, 279, 162 USPQ

221, 223 (CCPA 1979) (holding "interbonded by interfusion" to limit structure of the claimed composite and noting that terms such as "welded," "intermixed," "ground in place," "press fitted," and "etched" are capable of construction as structural limitations.) ~ *Extracted from M.P.E.P. 2113* ~

==========

Under the rule on M.P.E.P. 2113, it is believed that the structure of "electroplated copper" implied by a process step should be considered because "electroplated copper" can be expected to impart distinctive structural characteristics to the final product in the grain size using a TEM cross-section or in the composition analysis using Energy-Dispersive X-ray (EDX) spectroscopy or X-ray fluorescence.

Furthermore, both Lin and Nakanishi et al. fail to teach, hint or suggest the claimed subject matter that electroplated copper is between a solder contact and a contact pad comprising a gold layer with a thickness greater than 1 micrometer, as currently claimed in Claim 9.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 9 is respectfully requested.

Applicants respectfully submit independent Claim 9 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 10-12, 98, 99 and 118-122 patentably define over the prior art as well.

Response to Claims 15, 17-19, 21, 22, 25, 27, 29, 30, 101-103 and 108-112

==========

As currently amended, independent Claim 15 is recited below:

15. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, and wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening;
a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening;
a third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein the position of said third contact pad from a top perspective view is different from that of said first contact point, and wherein said third contact pad has a region used to be wirebonded thereto for connection made to a next level of packaging;
a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening;
a capacitor over said first polymer layer and over said second contact point; and
a solder contact between said second contact point and a terminal of said capacitor, wherein said solder contact connects said terminal to said second contact point.

==========

Reconsiderations of Claims 15, 17-19, 21, 22, 25, 27, 101-103 and 108-112 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 15 patentably distinguishes over the citation by Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980).

The Examiner considers that "It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi as above to include the claimed third contact pad for wirebonding and its location, such as the position of said third contact pad from a top perspective view is different from that of said first contact point. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a third contact pad that is closer to the periphery of the semiconductor substrate compared to the capacitor (which allows flexibility of placing the capacitor in a central location on the semiconductor substrate, as shown in Figure 3b of Nakanishi), while still being able to connect to the next level of packaging without excessive wirebond length." ~ *See line 20 of page 16 through line 7 of page 17, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion because there is no motivation to make Lin's capacitor 54 to be connected to a wirebond through a routing interconnect in view of Nakanishi et al.'s teaching. Nakanishi et al.'s capacitor 8 is an external capacitor having two terminals connected to an external circuitry through Nakanishi et al.'s wiring traces 5. However, Lin's capacitor 54 is an internal capacitor having two terminals both connected down to underlying devices through two openings in a passivation layer 18, but not to an external circuitry. The two terminals of Lin's capacitor

54 are suggested to be directly over contact points at bottoms of the two openings in the passivation layer 18 without any rerouting trace because this is the minimum connection to the underlying devices. Therefore, Nakanishi et al.'s wiring traces 5 or Nakanishi et al.'s wirebonding wires 12 are not believed to be applied to Lin's device because Lin fails to teach, hint or suggest Lin's capacitor 54 is an external capacitor, like Nakanishi et al.'s capacitor 8, having at least a terminal connected to an external circuitry.

Furthermore, Nakanishi et al. teach that a contact pad having a region used to be wirebonded thereto for connection made to a next level of packaging 17 or 15 is connected to a contact point 3 at a bottom of an opening in a lower insulating layer 4. The contact pad is directly over a contact point 3 at a bottom of an opening in a lower insulating layer 4, and the position of the contact pad from a top perspective view is the same as that of the contact point 3. However, Nakanishi et al. fail to teach, hint or suggest the claimed subject matter that a third contact pad having a region used to be wirebonded thereto for connection made to a next level of packaging is connected to a first contact point at a bottom of a first opening in a passivation through the first opening, and the position of the third contact pad from a top perspective view is different from that of the first contact point, as currently claimed in Claim 15.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 15 is respectfully requested.

Applicants respectfully submit independent Claim 15 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 17-19, 21, 22, 25, 27, 29, 30, 101-103 and 108-112 patentably define over the prior art as well.

Response to Claims 129-139

==========

As currently amended, independent Claim 129 is recited below:

129. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and on said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a first contact pad over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, and wherein said passivation layer comprises a nitride;
a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact point, and wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer;
a capacitor over said passivation layer and over said second contact pad;
a solder contact between a terminal of said capacitor and said second contact pad, wherein said solder contact connects said terminal to said second contact pad; and
a third contact pad between said solder contact and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold.

==========

Reconsiderations of Claims 129-139 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip currently claimed in amended Claim 129 patentably distinguishes over the citation by Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi et al. (U.S. Pat. No. 6,921,980).

The Examiner considers that "As for the thickness of the gold layer is considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer ....." ~ *See lines 1-7 on page 12, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion because a gold layer having a thickness greater than 1 micrometer is not believed to involve routine optimization. If the Examiner does consider that a gold layer having a thickness greater than 1 micrometer involves routine optimization, showing a reference disclosing the routine optimization of a gold layer having a thickness greater than 1 micrometer is respectfully requested.

The Examiner considers that "Lin (refer to Figure 10) also teaches a third contact pad (pad to which 52 is attached) between said solder contact (52) and said second contact pad, but does not specifically state that said third contact pad is "finished with solder wettable material comprising gold". However, given that this is a well known configuration in the art to improve solder wettability and 52 comprises solder, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that said third contact pad is finished with solder wettable material comprising gold. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a solder wettable coating that also provides good corrosion resistance prior to soldering." ~ *See line 15 of page 19 through line 7 of page 20, in the last Office Action mailed May 12, 2009* ~

Applicant respectfully traverses the Examiner's opinion. If the Examiner considers that a contact pad finished with a solder wettable material comprising gold is well known, showing evidence is respectfully requested.

Also, both Lin and Nakanishi et al. fail to teach, hint or suggest that a third contact pad between a second contact pad comprising a first gold layer with a thickness greater than 1 micrometer and a solder contact is finished with a solder wettable material comprising gold, as currently claimed in Claim 129.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 129 is respectfully requested.

Applicants respectfully submit independent Claim 129 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 130-139 patentably define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Arora not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761